



## Interleaved Buck and Boost Converter for Solar Applications

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**ABSTRACT** Solar Energy is the prominent source of renewable energy. But, it is unpleasant that, only partial amount of energy can be extracted from the Solar cells by our conventional DC-DC Boost converters. An interleaved buck and boost dc/dc converter is developed featuring smaller input/output filters, faster dynamic response and lower device stress than conventional designs, for solar powered applications. Input and output ripples of voltage and current of the converter is very low. The simulations were carried out using MATLAB/SIMULINK software package and hardware implemented.

**ARTICLE HISTORY** Received 13 June 2018 Revised 12 September 2018 Accepted 20 September 2018

**KEY WORDS** Interleaved converter, boost converter, solar, ripple.

### 1. Introduction

As the demand of power is gradually increasing day-by-day, one of the suitable best alternatives is choosing non-conventional sources like solar energy as the primary sources for power generation in power stations. Solar power which is several times greater than the one, which we are using at the present. Solar energy is capable of solving the grievance of global warming and energy thrust caused by the increase of energy consumption.

To enable the solar cell and to use sunlight efficiently, DC-DC converters are used for the solar power generation. But, the constraint is that DC-DC converters cannot extract 100% energy from the solar cell. Though, many techniques have been invented and implemented still, there is a lag and restrictions in the research of boost converters. Interleaving technique being an evolving technique, it can be a solution for the aforementioned problem

### 2. Solar Panel Design For Buck And Boost

The model of a solar cell shown Figure 1 is designed with all losses into account. The optical loss of the solar cell is represented by the input current source (Is). The recombination losses are represented by diode (D) which connected parallel to Is and the ohmic losses are represented by the shunt resistance (Rsh) and series resistance (Rs). Rs should be as low as possible because it is nothing but the sum of all resistance in the current path.

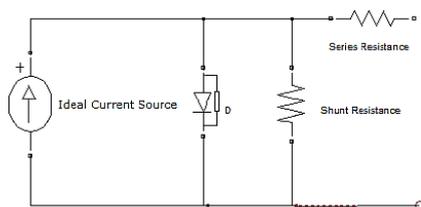


Fig. 1. Solar Model

The efficiency of a solar cell depends mainly on Short circuit current (Isc), open circuit voltage (Voc), Fill factor (FF). Best value of a good solar cell should be  $\geq 0.80$ .

$$FF = [V_{oc} - I_n (V_{oc} - 0.72)] / [V_{oc} + 1];$$

$$V_{oc} = [kT/q] * [\ln (I_1 / I_0) + 1];$$

Where,  $I_0 \rightarrow$  Recombination current in the material due to the electron-hole pair;

$I_1 \rightarrow$  Light generated current;

$V_{oc} \rightarrow$  Maximum voltage obtained when solar cell is left open;

$I_{sc} \rightarrow$  Maximum current when the solar cell terminals are shorted.

A buck converter is one which steps down voltage from its input to its output. The solar cell with boost converter, which is designed to produce an output voltage of 24.78V. In

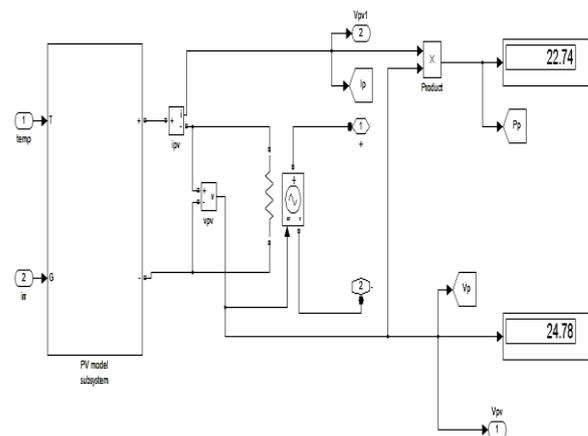


Fig. 2. Solar output for Buck mode

Figure 2, a simple buck converter is shown where the input of the converter is a solar cell.

A boost converter is one which gives increased output than the given input. The solar cell, which is designed to produce an output voltage of 48.67V. In Figure 2, a simple buck converter is shown where the input of the converter is a solar cell.

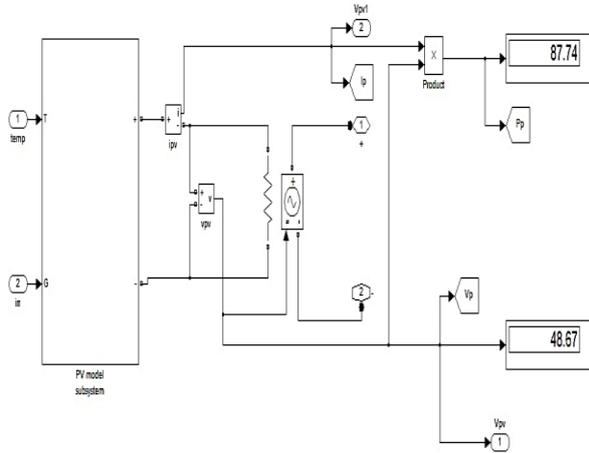


Fig. 3. Solar output for Boost model

**Mode 1:(boost)**

Boost mode is achieved when switches 3 and 4 ( $Q_3$  and  $Q_4$ ) turn on permanently and switches 1 and 2 ( $Q_1$  and  $Q_2$ ) operate with PWM signals.

**Mode 2:(buck)**

In the buck mode,  $Q_1$  and  $Q_2$  turn off permanently, and  $Q_3$  and  $Q_4$  operate in PWM.

The PWM activation signals of  $Q_1$  and  $Q_2$  are similar to each other with a phase shift of  $T_s/2$  for catering the interleaved pattern. The output voltage is regulated around a desired value by adjusting the duty cycle of the switches (here 24V and 58V) in both operational modes. A damping network, connecting a capacitor and series resistor decays output voltage oscillations occurring during the transitions between the operating modes when the input voltage is near the output voltage.

The benefit of output voltage oscillation cancellation via the time and the frequency domain analyses. In addition, through increasing the number of interleaved phases in boost and buck stages, the proposed converter can be easily used as a modular converter being suitable for transferring high power density in applications such as individual storage systems and many others.

**Interval 1:** In this time interval,  $Q_1, Q_3$ , and  $Q_4$  are in conducting mode, causing the magnetizing inductor 1 to start saving energy and concurrently magnetizing inductor 2 to transfer its stored energy to the output load and inductors via  $D_2$ .

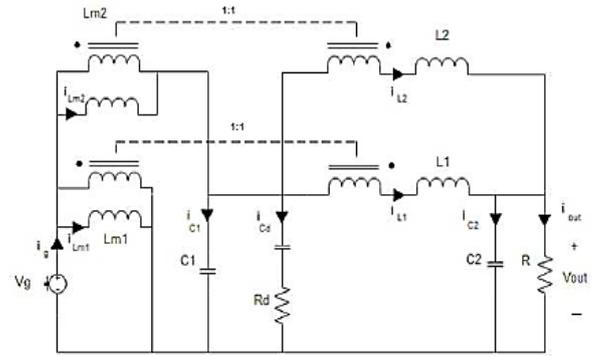


Fig. 4. During interval 1

**Interval 2 and 5:** In this time intervals,  $Q_3$  and  $Q_4$  are in conducting mode, while  $Q_1$  and  $Q_2$  turn off. Therefore, the energy stored in magnetizing inductors 1 and 2 starts transferring to inductors 1 and 2 via  $D_1$  and  $D_2$ . Similarly, a set of differential equations can be found for describing the voltage across the capacitors and current passing through the inductors for other time intervals. The differential equations describing the voltage across the capacitors and current passing through the inductors in these time intervals can be obtained as in interval 1.

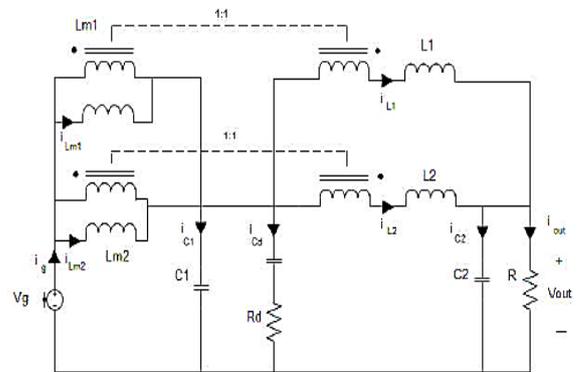


Fig. 5. During interval 2 and 5

**Interval 3:** In this time interval,  $Q_3$  is in conducting mode, while  $Q_1, Q_2$ , and  $Q_4$  are off. The energy transfer in this interval is completely similar to the previous interval except that the energy stored in both input magnetizing inductors is transferred to inductor 1 only.

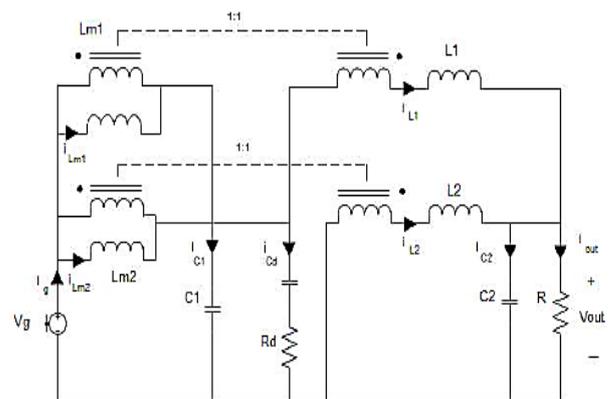
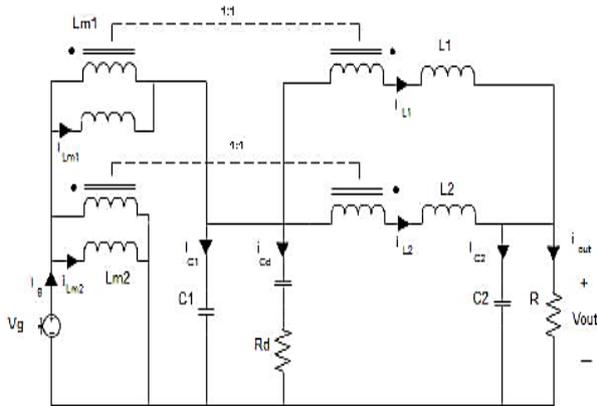


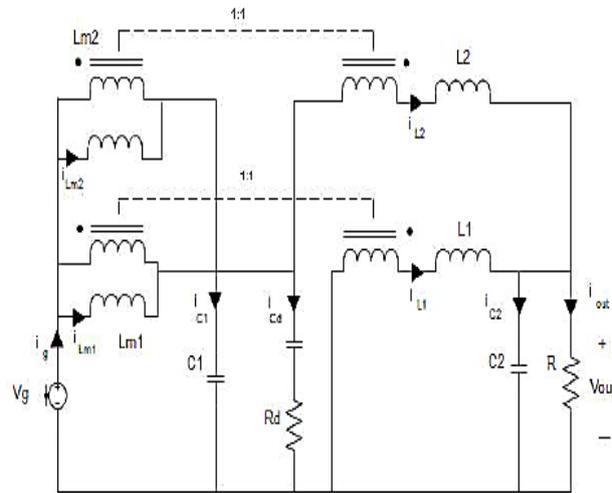
Fig. 6. During interval 3

**Interval 4:** In this time interval,  $Q_2, Q_3$ , and  $Q_4$  are in conducting mode, while  $Q_1$  is off. The energy transfer in this interval is also similar to that of interval 1 except that the functions of magnetizing inductors 1 and 2 replace each other.



**Fig. 7. During interval 4**

**Interval 6:** In this time interval,  $Q_4$  is in conducting mode, while  $Q_1, Q_2$ , and  $Q_3$  are off. Therefore, the energy stored in magnetizing inductors 1 and 2 is transferred to the output capacitor and inductor 2.



**Fig. 8. During interval 6**

### 6. Selection Of Buck-Boost Power Stage

The interleaved boost converter design involves the selection of the inductors, the input and output capacitors, the power switches and the output diodes. Both the inductors and diodes should be identical in both channels of an interleaved design. In order to select these components, it is necessary to know the duty cycle range and peak currents. Since the output power is channeled through two power paths, a good starting point is to design the power path components using half the output power.

The following parameters are required to calculate the power stage component.

Voltage across the capacitor	- $V_{c1}, V_{c2}$
Change in inductor current	- $\Delta i_{L1}$ or 2

Input voltage	- $V_g$
Change in magnetizing current	- $\Delta i_{Lm1}$ or 2
Magnetizing inductance	- $L_{m1}, L_{m2}$
Time period	- $T_s$
Input voltage	- $V_g$
Output voltage	- $V_{out}$

### 5. Expression for Inductance and Capacitance

The nominal current for power inductor is referred commonly to self heating with DC current at the temperature of +40°C. DC Resistance.

Selection of power inductor with the minimum possible DC resistance is important after the calculated values for inductance L and inductor currents. The DC resistance value is useful in finding wire heating losses for minimizing the power loss of the inductor. Choosing higher inductance value leads to increase the value of DC resistance and lower inductance value leads to decrease the value of DC resistance. Preferably, use of shielded inductor with same inductance value leads to decrease the value of DC resistance. It is advisable to keep Electro Magnetic Compatibility (EMC) for critical applications, the shielding of power inductor avoids uncontrolled magnetic coupling due to air gap exists in the windings with adjacent conductor tracks or components. It is highly preferable for selecting power inductor of small size, high energy storage density and low DC resistance.

#### Magnetizing inductance $L_{m1}$ and $L_{m2}$

**Boost mode :** 
$$\frac{V_g D_{12} T_s}{\Delta i L_{m1 \text{ or } m2 \text{ boost}}}$$

**Buck Mode:** 
$$\frac{\Delta V_{c \text{ buck}} T_s}{16 \Delta i L_{m1 \text{ or } 2 \text{ buck}}}$$

#### Inductance $L_1$ and $L_2$ :

**Boost mode :** 
$$\frac{V_g D_{12} T_s}{\Delta i L_{m1 \text{ or } m2 \text{ boost}}}$$

**Buck mode:** 
$$\frac{(V_g - V_{out}) D_{34} T_s}{\Delta i L_{m1 \text{ or } 2 \text{ buck}}}$$

Best practice is to use low Equivalent Series Resistance (ESR) capacitors to minimize the ripple on the output voltage. Ceramic capacitors are a good option if the dielectric material is X5R or better.

#### Capacitance $C_1$ :

**Boost mode :** 
$$\frac{V_{out}}{R} \frac{D_{12}}{(1 - D_{12})} \frac{(1 - 2D_{12}) T_s}{\Delta V_{c \text{ boost}} 2}$$

**Buck mode :** 
$$\frac{V_{out}}{R} \frac{(D_{34} - 1)(2D_{34} - 1)(T_s)}{\Delta V_{c \text{ buck}} 2}$$

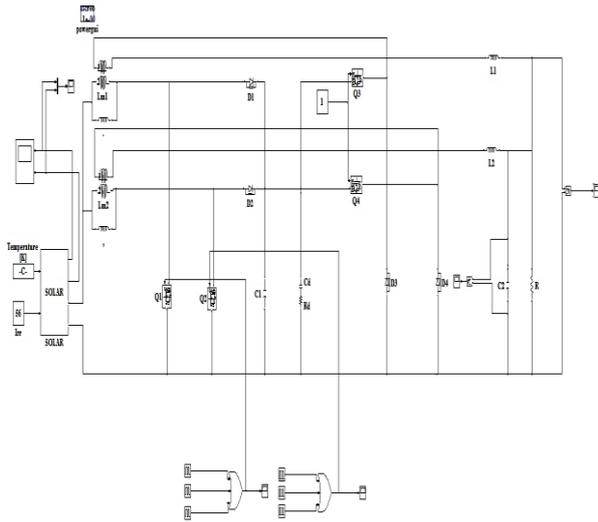
Capacitance  $C_2$  :

**Boost mode :** 
$$\frac{1}{32} T_s \Delta i_{Lm1 \text{ or } 2 \text{ boost}} / \Delta V_{c2 \text{ boost}}$$

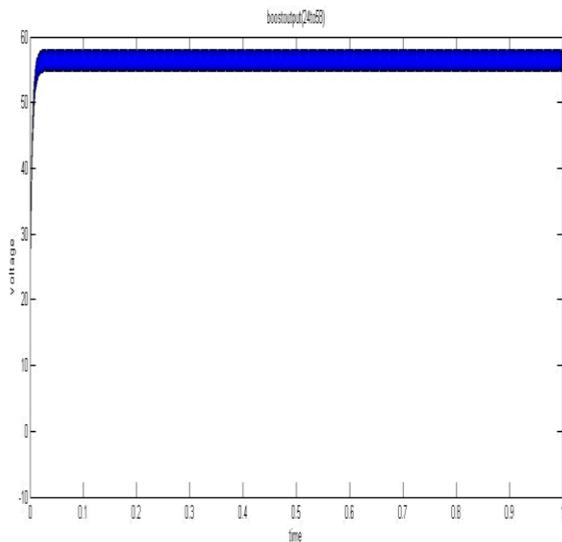
**Buck mode :** 
$$\frac{1}{32} T_s \Delta i_{L1 \text{ or } 2 \text{ buck}} / \Delta V_{c2 \text{ buck}}$$

**6. Results and Discussions**

The schematic diagram and output for the boost mode is shown in Figure 9 and Figure 10.

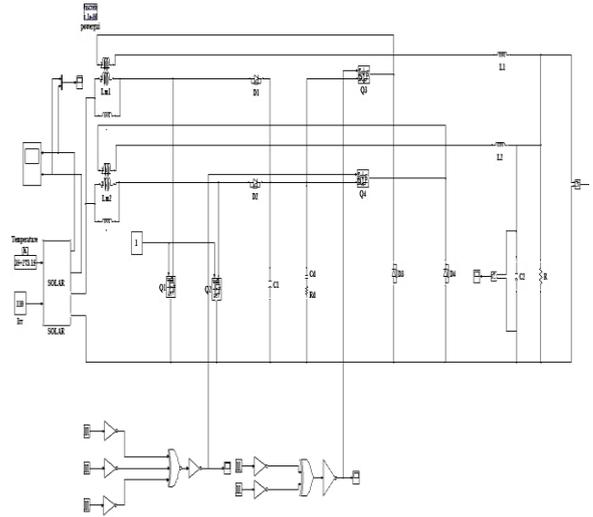


**Fig. 9. Simulation diagram for boost mode**

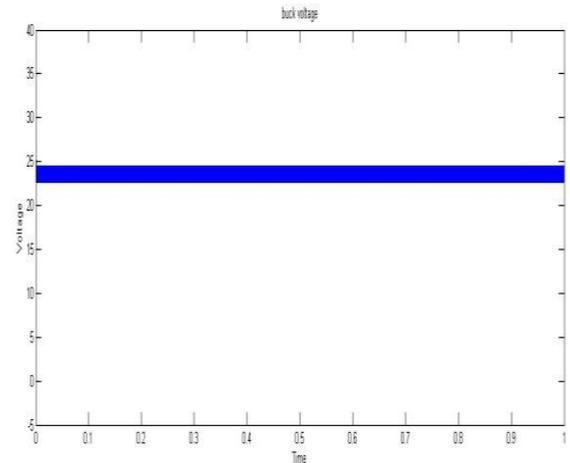


**Fig. 10. Simulation output for boost mode**

The schematic diagram and output for the buck mode is shown in figure 11 and figure 12.

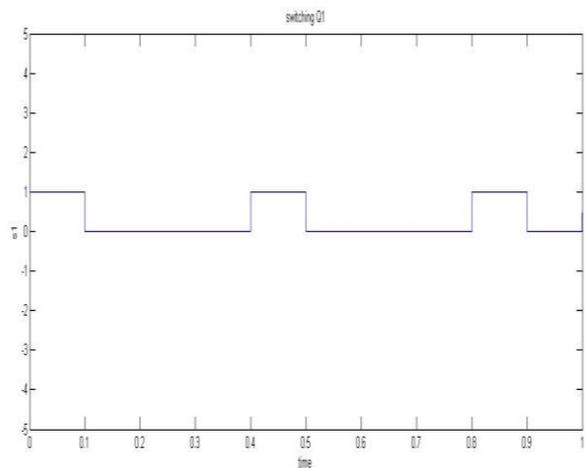


**Fig. 11. Simulation diagram for buck mode**



**Fig. 12. Simulation Output for buck mode**

The switching pattern Q1, Q2, Q3 and Q4 for buck and boost mode operation is shown in figure 13, 14, 15, 16.



**Fig. 13. Switching pattern Q1**

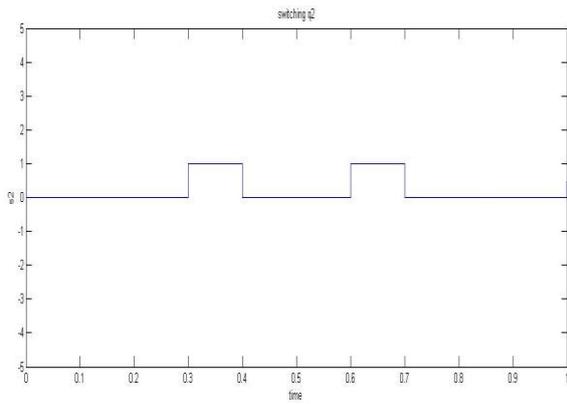


Fig. 14. switching pattern for Q2

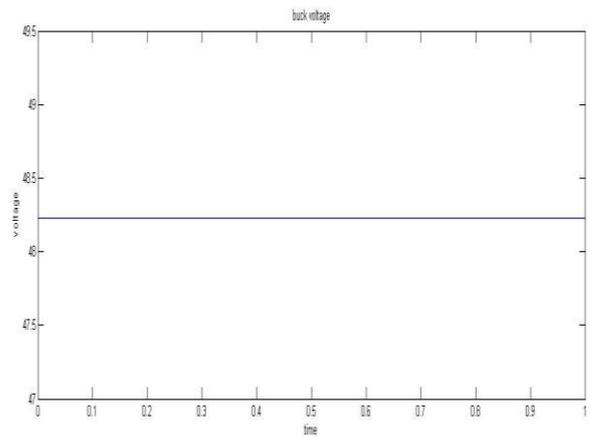


Fig. 17. Output for boost mode

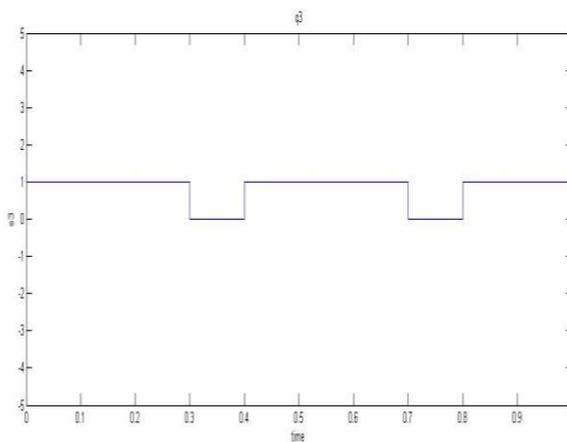


Fig. 15. Switching pattern for Q3

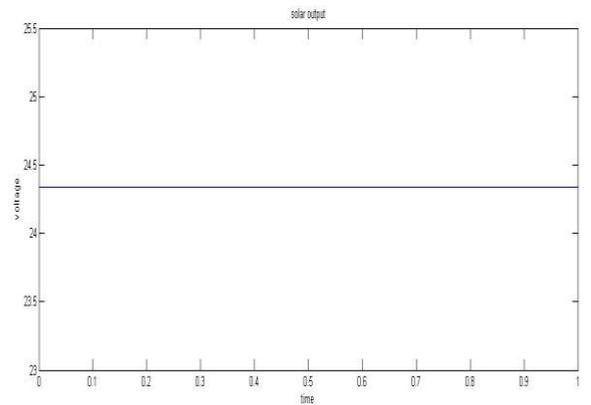


Fig. 18. Output for boost mode

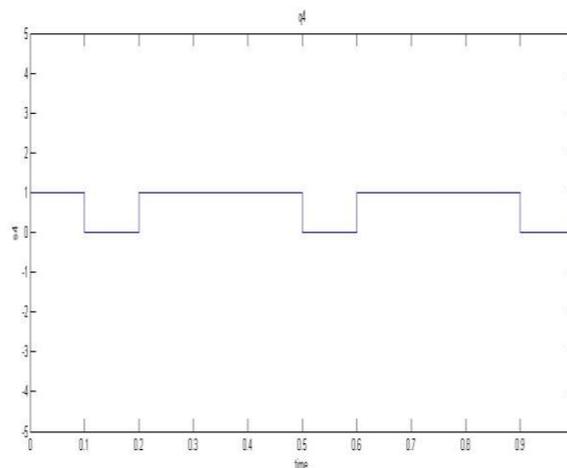


Fig. 16. Switching pattern for Q4

### SOLAR OUTPUT

The output of the solar with boost and buckmode with its transient is shown in Figure 17 and Figure 18.

### 7. Conclusion

Thus the given interleaved technique based buck and boost dc-dc converter has very low I/O current ripples with a very high efficiency. This simulation technique can utilized to select appropriate components for the converter. The circuit are simulated using MATLAB/Simulink. Finally, the results indicate that the efficiency of the proposed solution is higher than the conventional solution under the same condition.

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